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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,517	09/24/2001	Hitoshi Aoki	900-400	7216
23117	7590	10/03/2003	EXAMINER	
NIXON & VANDERHYE, PC 1100 N GLEBE ROAD 8TH FLOOR ARLINGTON, VA 22201-4714			THOMAS, TONIAE M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/960,517

Applicant(s)

AOKI, HITOSH

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12, 18, 20 and 22-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8, 9, 11, 12, 18, 20, 22, 23, 26 and 27 is/are rejected.
- 7) ☒ Claim(s) 7, 10, 24 and 25 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

DETAILED ACTION

*Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 August 2003 has been entered.
2. Currently, claims 1-12, 18, 20, and 22-27 are pending.

*Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. *Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

Claim 11 recites the limitation "wherein the second electrode entirely covers the first electrode and...or disposed only on the first electrode having a smaller size than the first electrode." It is unclear how the second electrode can be disposed only on the first electrode and have a smaller size than the first electrode, when independent claim

1 recites the limitation "wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at least one of the impurity regions" (claim 1, lines 12-14).

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. *Claims 1, 4-6, 11, 12, 18, 20, 22, 26, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Fournel et al. (US 2001/0019163 A1).*<sup>1</sup>

The Fournel et al. patent (Fournel) discloses a semiconductor device (figs. 3A-3c and par. [0044] to par. [0057]). The device comprises: a semiconductor substrate 1 of a first conductivity type (fig. 3A); a first electrode 205 provided on the semiconductor substrate with the intervention of a gate insulation film 207 (fig. 3A); a second electrode 211 provided at least on the first electrode with the intervention of an intermediate

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<sup>1</sup> Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

insulation film 209 (fig. 3A); at least a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region 215, an intermediate concentration impurity region 216, and a high concentration impurity region 217 sequentially arranged in this order from a region located underneath at least one of the first and second electrodes (fig. 3A); wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at least one of the impurity regions with intervention of the intermediate insulating film (fig. 3A); and wherein the high concentration impurity region 217 is laterally offset from and laterally spaced from the low concentration impurity region in the at least one impurity region (fig. 3A).

A sidewall insulation film 213 is provided on the sidewalls of the second electrode (fig. 3A).

The pair of impurity regions of the second conductivity type each include the low concentration impurity region 215, the intermediate concentration impurity region 216, and the high concentration impurity region 217 sequentially arranged in this order from the region located underneath the first electrode (fig. 3A).

The intermediate concentration impurity region is partly surrounded by the low concentration impurity region (fig. 3A).

The second electrode entirely covers the first electrode and further extends to one side or opposite sides of the first electrode on the semiconductor substrate (fig. 3A).

The first electrode and the second electrode serve as a-floating gate electrode and a control gate electrode, respectively, of a memory (par. [0025]).

The second electrode extends laterally beyond an edge of the first electrode so that the second electrode overlaps each of the first electrode and at least part of said low concentration impurity region and said intermediate concentration impurity region of at least one of said impurity regions of the second conductivity type (fig. 3A).

5. *Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Liu (US 5,202,576).*

Liu discloses a semiconductor device (). The device comprises: a semiconductor substrate 12 of a first conductivity type (fig. 2a); a first electrode 24 provided on the semiconductor substrate with the intervention of a gate insulation film 26 (fig. 2a); a second electrode 30 provided at least on the first electrode with the intervention of an intermediate insulation film 32 (fig. 2a); a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region 38 (fig. 2c), an intermediate concentration impurity region 40 (fig. 2d), and a high concentration impurity region 16 (fig. 2e) sequentially arranged in this order from a region located underneath at least one of the first and second electrodes (col. 5, lines 1-35); wherein an overlapping width of the first electrode 24 and a first one of the pair of impurity regions of the second conductivity type is different than an overlapping width of the first electrode and a second one of the pair of impurity regions of the second conductivity type (fig. 2e); and wherein the high concentration impurity region 16 is laterally offset

from and laterally spaced from the low concentration impurity region 38 in the at least one impurity region (fig. 2e).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. *Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fournel.*

Fournel does not teach the claimed ranges for the concentration and depth of low, intermediate, and high concentration impurity regions. However, the claimed ranges would have been obvious to one of ordinary skill in the art at the time the invention was made, since it has been held that where the general conditions of a claim are disclosed on the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

7. *Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fournel et al. in view of Su et al. (US 6,133,096).<sup>2</sup>*

Fournel further discloses forming a silicide layer on the first electrode 205 and the second electrode 211 (fig. 3C and par. [0048], lines 1-4). While Fournel discloses

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<sup>2</sup> The Su et al. patent was relied upon in the previous Office action.

forming a silicide layer on the first and second electrodes, Fournel does not teach forming a silicide layer on the high concentration impurity region.

Su et al. (Su) discloses a flash memory device, which comprises a floating gate 7b and a control gate 10, 11 (fig. 7B), and a pair of impurity regions (see. fig. 11). The impurity regions comprise a low concentration impurity region 17, an intermediate concentration impurity region 20, and a high concentration impurity region 23. A silicide layer 24 is formed on the high concentration impurity regions 23 (fig. 12).

Since both Fournel and Su are from the same field of endeavor, the purpose disclosed by Su would have been recognized in the pertinent art of Fournel by one of ordinary skill in the art at the time the invention was made.

One having ordinary skill in the art would have been motivated to modify Fournel by provided a silicide layer on the high concentration impurity region, as taught by Su, because the silicide layer lowers the contact resistance of the impurity region.

*Allowable Subject Matter*

8. Claims 7, 10, 24, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703)



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305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

*JMJ*

21 September 2001

  
AMIR ZARABIAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800